

**AMENDMENTS TO THE SPECIFICATION:**

Please amend the paragraph beginning on page 4, at line 6 as follows:

As shown in FIG. 2, the semiconductor chip 220 is mechanically and electrically interconnected to the chip contact pads 212 on the substrate ~~[[220]]~~ 210 via a plurality of solder joints 222. Since there is a significant difference between the substrate 210 and the semiconductor chip 220 in coefficient of thermal expansion (CTE) (a semiconductor chip typically has a CTE of about 3-5 parts per million per degree Celsius (ppm/°C) while a substrate typically has a CTE of about 20-30 ppm/°C), an underfill 230 is preferably provided between the substrate 210 and the semiconductor chip 220 for sealing voids formed among the solder joints 222. The underfill 230 provides stress relief in the solder joints 222 wherein the stress is caused by CTE mismatch between the semiconductor chip 220 and substrate 210.